Keysight N5399C/D HDMI HEAC Compliance Application

KEYSIGHT TECHNOLOGIES

Programmer's Reference

Notices

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In This Book

This book is your guide to programming the Keysight Technologies N5399C/D HDMI HEAC Compliance Application.

- Chapter 1, “Introduction to Programming,” starting on page 7, describes compliance application programming basics.
- Chapter 2, “Configuration Variables and Values,” starting on page 11, Chapter 3, “Test Names and IDs,” starting on page 31, and Chapter 4, “Instruments,” starting on page 49, provide information specific to programming the N5399C/D HDMI HEAC Compliance Application.

How to Use This Book

Programmers who are new to compliance application programming should read all of the chapters in order. Programmers who are already familiar with this may review chapters 2, 3, and 4 for changes.

Contents

1 Introduction to Programming

This chapter introduces the basics for remote programming a compliance application. The programming commands provide the means of remote control. Basic operations that you can do remotely with a computer and a compliance app running on an oscilloscope include:

- Launching and closing the application.
- Configuring the options.
- Running tests.
- Getting results.
- Controlling when and were dialogs get displayed
- Saving and loading projects.

You can accomplish other tasks by combining these functions.

Remote Programming Toolkit

The majority of remote interface features are common across all the Keysight Technologies, Inc. family of compliance applications. Information on those features is provided in the N5452A Compliance Application Remote Programming Toolkit available for download from Keysight here: "www.keysight.com/find/scope-apps-sw". The N5399C/D HDMI HEAC Compliance Application uses Remote Interface Revision 3.40. The help files provided with the toolkit indicate which features are supported in this version.

In the toolkit, various documents refer to "application-specific configuration variables, test information, and instrument information". These are provided in Chapters 2, 3, and 4 of this document, and are also available directly from the application's user interface when the remote interface is enabled (View>Preferences::Remote tab::Show remote interface hints). See the toolkit for more information.

Licensing

To enable programming of compliance applications on your oscilloscope, please visit "www.keysight.com/find/scope-apps" to purchase an N5452A remote programming option license.

2 Configuration Variables and Values

The following table contains a description of each of the N5399C/D HDMI HEAC Compliance Application options that you may query or set remotely using the appropriate remote interface method. The columns contain this information:

- GUI Location – Describes which graphical user interface tab contains the control used to change the value.
- Label – Describes which graphical user interface control is used to change the value.
- Variable – The name to use with the SetConfig method.
- Values – The values to use with the SetConfig method.
- Description – The purpose or function of the variable.

For example, if the graphical user interface contains this control on the **Set Up** tab:

- Enable Advanced Features

then you would expect to see something like this in the table below:

Table 1 Example Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Set Up	Enable Advanced Features	EnableAdvanced	True, False	Enables a set of optional features.

and you would set the variable remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SetConfig 'EnableAdvanced' 'True'"

C# syntax
```

```
---------
remoteAte.SetConfig("EnableAdvanced", "True");
```

Here are the actual configuration variables and values used by this application:

NOTE Some of the values presented in the table below may not be available in certain configurations. Always perform a "test run" of your remote script using the application's graphical user interface to ensure the combinations of values in your program are valid.

NOTE The file, ""ConfigInfo.txt"", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 2 Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Confgure	# Data-Data Edges	NumEdgeSkew	(Accepts user-defined text), 1, 2, 3, 4, 5, 6, 7, 8, 9, 10	Specifies the number of edges to use when performing the Data Data Inter-Pair Skew measurements. Increasing # Edges will increase run time but will improve repeatability.
Confgure	ARC Clock Frequency, Mhz	ARCFrequency	(Accepts user-defined text), 0, 4.096, 5.6448, 6.144	Specify the frequency for Audio Return Channel in Mhz.
Confgure	ARC Clock Recovery Loop Bandwitdth, HZ	ARCCRLoopBandwidth	(Accepts user-defined text), 700, 1500, 3000	Specify the loop bandwith required to recover clock of ARC signals.
Confgure	ARC Jitter Length, ms	ARCJitterLength	(Accepts user-defined text), 1, 25, 100, 1000	Specify the minimum waveform length in miliseconds for ARC jitter measurements.
Confgure	ARC Memory Depth	ARCMemoryDepth	(Accepts user-defined text), 10.00E+6, 8.00E+6, 2.05E+6, 1.025E+6, 524.288E+3, 262.144E+3, 32.768E+3	Define the memory depth for ARC tests.
Confgure	ARC Rise/Fall Time Edges	ARCRiseFallEdges	(Accepts user-defined text), 1000, 500, 100	Specifies minimum number of edges required for transition time measurement of ARC signals.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	ARC Sample Rate, MSa/s	ARCSRate	(Accepts user-defined text), 1000, 500, 250, 200	Specify the sample rate for ARC Tests in MSa/s.
Confgure	ARC Sampling Rate for Rise/FallTime, MSa/s	ARCRiseFallSamplingRate	(Accepts user-defined text), 1000, 5000, 10000, 20000	Specify the sampling rate required to measure rise/fall time.
Confgure	Additional Guard Band Pattern	GuardBandpattern	(Accepts user-defined text), Auto, 1101010100, 0010101011	This field allows you to enter additional Guard Band pattern to search, besides the default pattern. You can only enter digit 0 and 1 here. It needs to be 10 bits. 6 of these bits must consist of alternating 1s and 0s .The application use the default pattern only when None is selected. If you have more than one pattern to enter use ',' to separate them (example 0101010100,1010101011).
Confgure	Additional Sync Pattern	pattern	(Accepts user-defined text), Auto, 1101010100, 0010101011	This field allows you to enter additional pattern to search, besides the default pattern. You can only enter digit 0 and 1 here. It needs to be 10 bits. 6 of these bits must consist of alternating 1s and 0s .The application use the default pattern only when None is selected. If you have more than one pattern to enter use ',' to separate them (example 0101010100,1010101011).
Confgure	Cable Eye Measurement Setup Steps	SkipCableEyeSteps	false, true	Allows user to skip steps that perform signal autoscale, mask loading etc and go straight to mask test. User must perform a full mask test at least once in order to skip steps in subsequent runs.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	Cable Test Acquisition Points (Eye)	AcqPointCable	(Accepts user-defined text), 1000000, 10000000, 16000000	Specifies the number of accumulate points to measure in the data eye pattern test. Note that increasing the number of points has a negative impact on the run time of the data eye pattern tests and peak-to-peak jitter.
Confgure	Cable Test Equalize Mode	EqCable	manual, IR_Seq_typeE_02_225, IR_Seq_typeE_05_225, IR_Seq_typeE_10_225, IR_EQ_2.3_742.5M, off	Specify the equalizer mode to use.(Cable Test)
Confgure	Cable Test Mask Movement	MovementTypeCable	FINDPASS, FIXED, FINDMARGIN, MANUAL	This field contains 4 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs. (2) Fixed Mask will not be moving, it only report Pass or Fail upon test. (3) Find Biggest Margin will search +/-0.5 UI horizontally to find the maximum margin of non-violation mask. (4) Manual mode will allow the user to move the mask manually during the eye test.
Confgure	Cable Test Mask Rev	MaskRevCable	RevB, RevA	Select revision of mask to test with the eye. Rev-A is used for HDMI CTS 1.2. Rev-B is used for HDMI CTS 1.3 (Cable Test)
Confgure	Cable Test Mask Type	MaskFileCable	HDMI-TP2.msk, HDMI-TP3.msk, HDMI-TP5.msk	Select type of mask to use in Eye Test.(Cable Test)
Confgure	Check Diff Probe	CheckDiffProbe	True, False	Turn off check on differential probing. For Debug purpose.
Confgure	Clock Check Max Std. Deviation (Mhz)	ClockCheckMaxStdDv	(Accepts user-defined text), 4.0, 2.0, 1.0	Set the maximum standard deviation tolerance for clock signal verification

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	Clock Duty Cycle Edges	NumEdgeClockDutyCycle	(Accepts user-defined text), 400, 1000, 10000	Specifies the number of edges to use when performing the Clock Duty Cycle measurements. Increasing # Edges will increase run time but will improve repeatability.
Confgure	Clock Duty Cycle Measurement Method	ClockDutyCycleMethod	(Accepts user-defined text), 1, 2	Defines measurement method for clock duty cycle test. For method "1", the duty cycle is measured by triggering on rising edge of the clock and measuring the mode of the falling edge after making n number of acquisitions. For method "2", only a single acquisition will be made and the duty cycle will be measured for the first 10000 edges using MATLAB analysis.
Confgure	Clock Jitter Acquisition Points	NumEgdeJitter	(Accepts user-defined text), 5000000, 10000000, 16000000	Specifies the number of accumulate points to use when performing the Clock Jitter measurements. Increasing # points will increase run time but will improve repeatability.
Confgure	Clock Jitter Measurement Setup Steps	SkipJitterSteps	false, true	Allows user to skip steps that perform signal autoscale and go straight to clock jitter test. User must perform a full clock jitter test at least once in order to skip steps in subsequent runs.
Confgure	Clock Jitter Multiplier	ClkJitterMultiplier	AUTO, 1, 5, EDGE	Determines the type of multiplier method used in recover clock.
Confgure	Clock Jitter Multplier (Cable)	ClkJitterMultiplierCable	AUTO, 1, 5, EDGE	Determines the type of multiplier method used in recover clock.(Cable Test)
Confgure	Clock Jitter Multplier (Receiver)	ClkJitterMultiplierReceiver	AUTO, 1, 5, EDGE	Determines the type of multiplier method used in recover clock.(Receiver Test)
Confgure	Clock Multiplier	ClkMultiplier	Auto, 10, 40	Select clock multiplier to use.
Confgure	D+ Channel	CableDataP	CHAN1, CHAN2, CHAN3, CHAN4	Identifies the oscilloscope channel that is probing +ve Intra-Pair Data Lane.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	D+ Channel	DataP	CHAN1, CHAN2, CHAN3, CHAN4, CHAN5	Identifies the oscilloscope channel that is probing Data Lane A.(Single-Ended Model)
Confgure	D- Channel	CableDataN	CHAN1, CHAN2, CHAN3, CHAN4	Identifies the oscilloscope channel that is probing -ve Intra-Pair Data Lane.
Confgure	DUT supports clock rates > 165MHz	SupportHighRates	true, false	Specifies whether the DUT supports clock rates > 165MHz. Lower limit for test ID 7-2 will be set to 2.7V if DUT does not support clock rates > 165MHz. Otherwise the VL lower limit will be set to 2.6V.
Confgure	Data Lane A	RptDataLane1	D0, D1, D2	Identifies the target data lane for measurement and reporting.
Confgure	Data Lane A Channel	Data1	CHAN1, CHAN2, CHAN3, CHAN4	Identifies the oscilloscope channel that is probing Data Lane A.(2 Channels Connection Model)
Confgure	Data Lane A Channel	Data1Cable	CHAN1, CHAN2, CHAN3, CHAN4	Identifies the oscilloscope channel that is probing Data Lane A.(2 Channels Connection Model)
Confgure	Data Lane B	RptDataLane2	D0, D1, D2	Identifies the target data lane for measurement and reporting. This field is used for Inter-Pair Skew - Data Lane A/Data Lane B only.
Confgure	Data Lane B Channel	Data2	CHAN1, CHAN2, CHAN3, CHAN4, CHAN5	Identifies the oscilloscope channel that is probing Data Lane B. This field is used for Inter-Pair Skew - Data Lane A/Data Lane B only. (2 Channels Connection Model)
Confgure	Data Lane B Channel	Data2Cable	CHAN1, CHAN2, CHAN3, CHAN4	Identifies the oscilloscope channel that is probing Data Lane B.(2 Channels Connection Model)
Confgure	Data Rate (Gb/s)	DataRate	(Accepts user-defined text), 2.25	This is the default Data Rate in Gb/s for the HDMI Testing.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	Data Rate For Clock Recovery	DataRateForClkRecovery	(Accepts user-defined text), 3400000000	Sets the custom data rate for clock recovery. This value will only be used when "Enabled Data Rate For Clock Recovery" option is set to true.
Confgure	Data rate measurement method	DataRateMeasMethod	1, 2	Choose the method to measure the data rate of the signal. For method 1, data rate is measured using ":MEASure:DATarate" with histogram turned on. The mode of the histogram is taken as the measured data rate. For method 2, data rate is measured using ":MEASure:CDRRATE". The clock recovery used in method 2 is "Constant Frequency, Semi-Automatic" where the nominal data rate is taken from the TMDS character rate set in the "Device Definition Setup" dialog. This method works better for signals with lots of ISI.
Confgure	DeEmbedTP1	DeEmbedTP1	1.0, 0.0	DeEmbedTP1
Confgure	Enabled Data Rate For Clock Recovery	EnabledDataRateForClkRecovery	true, false	Enable or disable custom data rate for clock recovery. Please set the data rate in the "Data Rate For Clock Recovery" option.
Confgure	Enhanced Bandwidth	bwreduction	AUTO, 4E9, 6E9, 8E9, 12E9, 13E9, 14E9, 15E9, 16E9, 17E9, 18E9, 19E9, 20E9, 21E9, 22E9, 23E9, 24E9, 25E9, 26E9, 27E9, 28E9, 29E9, 30E9, 31E9, 32E9	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available with Enhance Bandwidth or Noise Reduction options.
Confgure	External Triggering	EXTTRIGGER	NO, CHAN4, AUX	Specify if to use trigger from ParBERT.(Receiver Test)
Confgure	External Triggering	EXTTRIGGERCable	NO, CHAN4, AUX	Specify if to use trigger from ParBERT.(Cable Test)

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	Eye Diagram Acquisition Points	AcqPoint	(Accepts user-defined text), 1000000, 10000000, 16000000, 100000000	Specifies the number of accumulate points to measure in the data eye pattern test. Note that increasing the number of points has a negative impact on the run time of the data eye pattern tests and peak-to-peak jitter.
Confgure	Eye Diagram Interpolation	AcqInterp	ON, OFF	Specifies whether to turn on or off Sin(x)/x interpolation. Turning on interpolation will likely have more peak-to-peak jitter.
Confgure	Eye Diagram Mask Movement	MovementType	FINDPASS, FIXED, FINDMARGIN, MANUAL	This field contains 4 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs. (2) Fixed Mask will not be moving, it only report Pass or Fail upon test. (3) Find Biggest Margin will search +/-0.5 UI horizontally to find the maximum margin of non-violation mask. (4) Manual mode will allow the user to move the mask manually during the eye test, only work on TP1 masks.
Confgure	Eye Height Measurement Location	EyeHeightLocation	CenterEye, EntireEye	Select whether to measure eye height on center of eye or the entire eye. When measuring eye height on entire eye, the largest eye opening accross the entire eye is reported. This is mostly useful when the eye is not symmetrical. When measuring eye height at center of eye, the eye height opening reported is at the center of the eye only. This is mostly used for a symmetrical eye.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	Eye Location	EyeLoc	-1, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10	Specifies location of the eye in respective to rising edge of clock. Choose composite to let all data bit in pixel overlap each other. Choose worst eye to let the application automatically select the bit location within the pixel clock interval with the smallest margin.
Confgure	Eye Measurement Setup Steps	SkipEyeSteps	false, true	Allows user to skip steps that perform signal autoscale, mask loading etc and go straight to mask test. User must perform a full mask test at least once in order to skip steps in subsequent runs.
Confgure	Fall Trigger Pattern	FallTriggerPattern	110, 1110	Specifies the Pattern to use as trigger condition when performing the Rise/Fall measurements.
Confgure	HEAC Single-Ended Lane+	HEACSingleEndedLanePlus	CHAN1, CHAN2, CHAN3, CHAN4	Define scope channel for HEC differential lane.
Confgure	HEAC Single-Ended Lane-	HEACSingleEndedLaneMinus	CHAN1, CHAN2, CHAN3, CHAN4	Define scope channel for HEC differential lane.
Confgure	HEC Base Center Margin	HECBaseCenterMargin	(Accepts user-defined text), 15, 15	Specifies the maximum margin allowed to estimate of position base/center voltage in percentage to peak-to-peak voltage ratio .
Confgure	HEC Clock Recovery Loop Bandwidth, Khz	HECLoopBandwitdh	(Accepts user-defined text), 75, 1000	Specify loop bandwith for clock recovery.
Confgure	HEC Cycle Time Count	HECCycleTimeUI	(Accepts user-defined text), 10, 100, 1000	Specifies the number of measurements taken for cycle time tests.
Confgure	HEC Differential Lane	HECDifferentialLane	CHAN1, CHAN2, CHAN3, CHAN4	Define scope channel for HEC differential lane.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	HEC Eye Diagram Minimum UI	HECEyeMinUI	(Accepts user-defined text), 4000, 100000, 500000, 1000000	Specifies the number of accumulate points to measure in the data eye pattern test for HEC eye diagram test. Note that increasing the number of points has a negative impact on the run time of the data eye pattern tests and peak-to-peak jitter.
Confgure	HEC Jitter Cross Line	HECJitterCrossLine	(Accepts user-defined text), Auto, Manual	Auto/Manual setting of the cross line of HEC jitter test.
Confgure	HEC Level Measurements Count	HECLevelMeasurementCount	(Accepts user-defined text), 1, 10, 50, 100	Specifies number of measurement to be taken for High, Center and Low Level Test.
Confgure	HEC Memory Depth	HECMemoryDepth	(Accepts user-defined text), 2.05E+6, 1.025E+6, 524.288E+3, 262.144E+3, 32.768E+3	Define the memory depth for HEC tests.
Confgure	HEC Operating Voltage Count	HECOperatingVoltageCount	(Accepts user-defined text), 100, 50, 10	Specifies the number of measurements taken for operating voltage test.
Confgure	HEC Rise/Fall Time Edges	HECRiseFallEdges	(Accepts user-defined text), 10, 50, 100	Specifies minimum number of edges required for transition time measurement .
Confgure	HEC Sample Rate, GSa/s	HECSRate	(Accepts user-defined text), 40, 20, 10, 5	(Limited availability*) Specify the sample rate for HEC Differential Tests in GSa/s.
Confgure	HEC Top Center Margin	HECTopCenterMargin	(Accepts user-defined text), 15, 15	Specifies the maximum margin allowed to estimate of position top/center voltage in percentage to peak-to-peak voltage ratio.
Confgure	HEC Trigger Duration, UI	HECTriggerDuration	(Accepts user-defined text), 9, 10, 11, 12	Specifies the minimum duration for stable signals for High, Center and Low Level Test.
Confgure	HEC Window Trigger Method	HECWindowTriggerMethod	Hardware, Software	Define window trigger method for high, level and center level test. Hardware method improves speed performance but might not be fully supported in some scopes.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	Hide Informative Tests	HideInformativeTests	1.0, 0.0	Hides or shows informative test
Confgure	Hysteresis(+-mV)	CableMeasHys	(Accepts user-defined text), 10	Sets the threashold hysteresis.(Cable Test)
Confgure	Inter-Pair Measurement Trigger Wait (ms)	InterPairTriggerWait	(Accepts user-defined text), 3000, 5000, 7000, 10000, 30000, 50000, 70000, 100000, 150000, 200000, 300000, 500000	Defines wait time for inter-pair trigger.
Confgure	Inter-Pair Skew Method HDMI 1.4	InterpairMethod14	1, 2	Choose the method to measure inter-pair skew. For method 1, InfiniiScan is used to trigger on required pattern. For method 2, a large acquisition will be captured, then the required SYNC patterns will be searched throughout captured pattern.
Confgure	Inter-Pair Skew Method HDMI 2.0	InterpairMethod	1, 2	Choose the method to measure inter-pair skew. For method 1, InfiniiScan is used to trigger on required pattern. For method 2, a large acquisition will be captured, then the required SYNC patterns will be searched throughout captured pattern.
Confgure	Inter-Pair Skew Reference Channel	InterPairReferenceChannel	Clk, D2	Define the inter-pair skew reference channel when switch matrix is enabled.
Confgure	Inter-pair Skew Batch Size	InterPairBatSize	(Accepts user-defined text), 20.00E+6, 10.00E+6, 5.00E+6	Define the memory depth for Inter Pair Skew tests. For method 2 only.
Confgure	Inter-pair Skew Memory Depth	InterPairMemDepth	(Accepts user-defined text), 10.00E+6, 50.00E+6, 100E+6, 150E+6, 200E+6, 500E+6	Define the memory depth for Inter Pair Skew tests. For method 2 only.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	InterPair Skew Trigger Length	TriggerLength	20, 10	This field allow user to select 10 bits or 20 bits trigger pattern for inter-pair skew test.
Confgure	Intra-Pair Data Lane	CableIntraPairRptDataLane	D0, D1, D2	Identifies the target data lane for measurement and reporting.
Confgure	Intra-Pair Measurement Method	IntraPairMethod	1, 2	Defines measurement method for intra-pair skew test. For method "1", the skew is measured by setting channel A as trigger channel and measuring skew on channel B. Multiple acquisitions will be required for this acquisition. For method 2, only 1 acquisition is required and intra-pair skew is measured on each captured edge.
Confgure	Intra-Pair Skew Crossing Reference	IntraPairCrossingRef	LaneP, LaneN	Specifies the crossing-point reference for intra-pair skew test.
Confgure	Intra-Pair Skew Edges	NumEdgeIntraSkew	(Accepts user-defined text), 100, 1000, 10000	Specifies the number of edges to use when performing the Intra-Pair Skew measurements. Increasing # Edges will increase run time but will improve repeatability.
Confgure	Intra-Pair Skew Histogram Offset	IntraHistogramOffset	0, 1, 5, 10, 20, 30	Specifies the offset of Histogram threshold (in mV) for Skew measurement.
Confgure	Intra-Pair Skew Interpolation	IntraPairInterpolation	OFF, ON	Enabling or Disabling Interpolation.
Confgure	Jitter Seperation Memory Depth	RjDjMemoryDepth	(Accepts user-defined text), 2000000, 4000000, 8000000, 12000000	Define the memory depth per acquisition for Data Jitter Seperation tests.
Confgure	Mask Rev	MaskRev	RevB, RevA	Select revision of mask to test with the eye. Rev-A is used for HDMI CTS 1.2. Rev-B is used for HDMI CTS 1.3

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	Mask Type	MaskFile	HDMI-TP1.msk, HDMI-TP1.msk, HDMI-TP2.msk, HDMI-TP5.msk, HDMI-DP++.msk	Select type of mask to use in Eye Test.
Confgure	Maximum Tries	Maxtries	(Accepts user-defined text), 3, 5, 10, 50, 100	Specifies the maximum tries before timeout. This setting needed to be increase when testing at lower pixel rate.
Confgure	Measurement Threshold(V)	CableMeasThres	(Accepts user-defined text), 0	Sets the measurement threashold.(Cable Test)
Confgure	PC_IPAdress	PC_IPAdress	(Accepts user-defined text), None	PC_IPAdress.
Confgure	PC_Port	PC_Port	(Accepts user-defined text), None	PC_Port
Confgure	PC_ReceiveTimeout	PC_ReceiveTimeout	(Accepts user-defined text), None	PC_ReceiveTimeout
Confgure	PC_SendTimeout	PC_SendTimeout	(Accepts user-defined text), None	PC_SendTimeout
Confgure	Pattern Lane A	LaneAPatt	(Accepts user-defined text), Auto, 0010101011001010101011, 0010101010001010101010, 0010101011001010101011/0010101010001010101010, 0010101011001010101011/0010101010001010101010/1101010100110101010100	For HDMI 2.0 inter-pair skew only. Specify the pattern to use to trigger Lane A for method '1' or pattern to search for method '2'. If there are multiple patterns to try out, just use the '/' separator.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	Pattern Lane B	LaneBPatt	(Accepts user-defined text), Auto, 0010101011001010101011, 0010101011001010101011/0010101010010101010, 0010101011001010101011/0010101010010101010/1101010100110101010100	For HDMI 2.0 inter-pair skew only. Specify the pattern to search for in Lane B. Once the oscilloscope triggers on Lane A, the software will search Lane B for specified pattern. If there are multiple patterns to try out, just use the '/' separator.
Confgure	Pixel Clock(MHz)	CablePixClk	(Accepts user-defined text), 74.25, 340	Sets the pixel clock rate according to cable category.(Cable Test)
Confgure	Probe Check	ProbeCheck	Enable, Disable	Enable or disable probe check.
Confgure	Raw Clock Frequency	RawClockFreq	(Accepts user-defined text), auto, 222750000	Specify the raw clock frequency send by the transmitter.(Receiver Test)
Confgure	Raw Clock Frequency	RawClockFreqCable	(Accepts user-defined text), auto, 222750000	Specify the raw clock frequency send by the transmitter.(Cable Test)
Confgure	Receiver Eye Measurement Setup Steps	SkipReceiverEyeSteps	false, true	Allows user to skip steps that perform signal autoscale, mask loading etc and go straight to mask test. User must perform a full mask test at least once in order to skip steps in subsequent runs.
Confgure	Receiver Test Acquisition Points (Eye)	AcqPointReceiver	(Accepts user-defined text), 1000000, 10000000, 16000000	Specifies the number of accumulate points to measure in the data eye pattern test. Note that increasing the number of points has a negative impact on the run time of the data eye pattern tests and peak-to-peak jitter.
Confgure	Receiver Test Clock Channel	ClkChan	CHAN1, CHAN2, CHAN3, CHAN4	The scope channel used to probe transmitted clock from the DUT.(Receiver Test)

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	Receiver Test Data Channel	DataChan	CHAN1, CHAN2, CHAN3, CHAN4	The scope channel used to probe transmitted Data from the DUT.(Receiver Test)
Confgure	Receiver Test Equalizer Mode	Eq	auto, manual, IR_Seq_typeE_02_225, IR_Seq_typeE_05_225, IR_Seq_typeE_10_225, IR_Seq_typeE_10_225, IR_EQ_2.3_742.5M, off	Specify the equalizer mode to use.
Confgure	Rise Trigger Pattern	RiseTriggerPattern	001, 0001	Specifies the Pattern to use as trigger condition when performing the Rise/Fall measurements.
Confgure	Rise/Fall Threshold	RiseFallThreshold	90/10, 85/15, 80/20, 75/25, 70/30	Specifies the upper threshold in percentage. The value must be in range from 50 to 100.
Confgure	Rise/fall time method	RiseFallMethod	1, 0	Specifies the method used when performing the Rise/Fall Time measurements. 0 (default) will measure based on any edge. 1 will measure based on triggering on 0001/1110 edge.
Confgure	Set termination voltage for N4444A probe head	EnableN5444Termination	True, False	If using N5444A probe head, select whether to let the application set the 3.3V termination automatically. If set to "false", the application will not set the internal termination voltage.
Confgure	Skip Connection PopUp	SkipConnectionPopUp	true, false	Turn On/Off Offline mode.
Confgure	Software Clock Recovery	SwCR	1st, 2nd	To specify which order of Software Clock Recovery to use.(Receiver Test)
Confgure	Store Detected Bits	StoreDetectedBits	No, Yes	Select whether to store detected bits for Lanes A and B. Bits will be stored in CSV format.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	TemplateFilePath	TemplateFilePath	(Accepts user-defined text), None	TemplateFilePath
Confgure	Termination Voltage	TerminationVoltage	(Accepts user-defined text), 3.3	Set termination voltage when infiniMax III probes are used.
Confgure	TestPlan Checkoff Mode	Demo	false, true	Skip tests and just run testplan
Confgure	Transition Time Converter Mode	TTCCable	SWTTCAUTO, SWTTCOFF, SWTTCMANUAL, TTC1, TTC2, TTC3, TTC4, TTC5, TTC6	Specify the Transition Time Converter mode to use. TTC Auto will automatically select the desired filter based on the channel frequency; TTC Off will disable the feature; TTC Manual allow user to determine the equ file manually during the test; TTC Model 1 will select 1200ps rise time, it should be chosen for freq <= 27Mhz; TTC Model 2 will select 450ps rise time, it should be chosen for freq = 74.25Mhz; TTC Model 3 will select 220ps rise time, it should be chosen for Freq = 148.5Mhz; TTC Model 4 will select 200ps rise time, it should be chosen for freq = 165Mhz; TTC Model 5 will select 150ps rise time, it should be chosen for freq = 222.25Mhz;TTC Model 6 will select 60ps rise time, it should be chosen for Freq > 222.75Mhz.
Confgure	Transmitter Sample Rate, GSa/s	TMDSSRate	40.0e+9, 20.0e+9	(Limited availability*) Specify the sample rate for Transmitter Tests in GSa/s.
Confgure	TurnOnCableEmbedding	TurnOnCableEmbedding	1.0, 0.0	TurnOnCableEmbedding
Confgure	TurnOnFixtureDeEmbed	TurnOnFixtureDeEmbed	1.0, 0.0	TurnOnFixtureDeEmbed
Confgure	TurnOnHDMIEqualizer	TurnOnHDMIEqualizer	1.0, 0.0	TurnOnHDMIEqualizer

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	TurnOnWorstCaseSkew	TurnOnWorstCaseSkew	1.0, 0.0	TurnOnWorstCaseSkew
Confgure	VL Edges	NumEdgeVL	(Accepts user-defined text), 100, 1000, 10000	Specifies the number of edges to use when performing the VL measurements. Increasing # Edges will increase run time but will improve repeatability.
Confgure	VL measurement method	VLMethod	1, 0	Specifies the method used when performing the VL measurements. 0 (default) will measure based on the any edge. 1 will measure based on triggering on 0001/1110 edge.
Confgure	Vswing Measure	VSwingCount	(Accepts user-defined text), 50, 100, 500, 1000	Specifies the number of Edges to use when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves repeatability of the measurement.
Run Tests	Event	RunEvent	(None), Fail, Margin < N, Pass	Names of events that can be used with the StoreMode=Event or RunUntil RunEventAction options
Run Tests	RunEvent=Margin < N: Minimum required margin %	RunEvent_Margin < N_MinPercent	Any integer in range: 0 <= value <= 100	Specify N using the 'Minimum required margin %' control.
Set Up	165Mcsc < TMDS Character Rate < 340Mcsc	PixelClockV130	0.0, 1.0	Set TMDS Character Rate to Between 165Mcsc and 340 Mcsc Set TMDS Character Rate to Between 165Mhz and 340 Mcsc
Set Up	CDF Path	CDFPath	(Accepts user-defined text)	File path for CDF
Set Up	Channel ConnectionType	HDMIConnectionType	1 Data Lane, 3 Data Lanes	Set the Connection Type Channel ConnectionType
Set Up	Check to Enable Automation	EnableHDMIAutomation	0.0, 1.0	Enable HDMI Automation Check to Enable Automation
Set Up	Check to Enable Automation	EnableHDMIAutomation	0.0, 1.0	Enable HDMI Automation Check to Enable Automation

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Comments	persistentTextbox1	(Accepts user-defined text)	Extra Comment field. This field will be reported in HTML report header.
Set Up	Connection Choice	ConnectionChoice	2 Probes, 4 Probes	Determined the connection choice whether Single-Ended or differential probes are being used.
Set Up	ConnectionSetupComplete	ConnectionSetupComplete	0.0, 1.0	Remotely specify whether connection setup complete
Set Up	DNModule	DNModule	(Accepts user-defined text)	DNModule
Set Up	DPModule	DPModule	(Accepts user-defined text)	DPModule
Set Up	DUTTimingSelection	DUTTimingSelection	Load from CDF, Load from Template, Manual Select	Determine type of tests to run.
Set Up	Device Definition Complete	DeviceDefinitionComplete	0.0, 1.0	Remotely specify whether device definition complete
Set Up	Device Identifier	DeviceID	Transmitter, Receiver, Cable	Determined Device Type is testing.
Set Up	Device Name	persDeviceName	(Accepts user-defined text)	Device name of the DUT being tested. This field will be reported at the HTML report header.
Set Up	Enable custom automation dll.	EnableCustomAutomation	0.0, 1.0	Enable custom automation dll.
Set Up	Enable custom automation dll.	EnableTestPlan	0.0, 1.0	Enable custom automation dll.
Set Up	FixtureType	FixtureType	N1080H04, High Z Probe, Wilder HDMI TPA-P, BitifEye Bit -1010-0200-0 Type A Adapter, Other	Fixture Type Fixture Type
Set Up	FlexEDIDVoltage	FlexEDIDVoltage	(Accepts user-defined text)	FlexEDIDVoltage
Set Up	HDMI Specs	HDMIRevision	2.0, 1.4b	Determine the HDMI Specification being tested.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	HDMI Test Type	HDMITestType	TMDS Physical Layer Tests, HEAC Tests, Direct Attach Tests	Determine type of tests to run.
Set Up	HDMIAutomationDriver	HDMIAutomationDriver	VPrime Flex EDID, PC LAN, QD 980	Select FlexEDID or PC LAN
Set Up	HEAC Test Mode	HEACTestMode	HEC, ARC (Common Mode), ARC (Single Mode), Both	Set the HEAC Test Mode.
Set Up	MaxTMDSCharRate	MaxTMDSCharRate	(Accepts user-defined text)	MaxTMDSCharRate
Set Up	MaxTMDSClock	MaxTMDSClock	(Accepts user-defined text)	MaxTMDSClock
Set Up	ProbeHeadType	ProbeHeadType	N5380A/B, N5444A	Probe Head Type
Set Up	QD980IP	QD980IP	(Accepts user-defined text)	QD980IP
Set Up	QDSlot	QDSlot	(Accepts user-defined text)	QDSlot
Set Up	SPDT6XModule	CDFPath	(Accepts user-defined text)	SPDT6XModule
Set Up	Show HEAC Tests.	ShowHEACTests	0.0, 1.0	Show HEAC Tests.
Set Up	SwitchMatrixStatus	SwitchMatrixStatus	On, Off	Determined whether switch matrix is being used.
Set Up	TMDS Character Rate >= 340 Mcsc	PixelClockV200	0.0, 1.0	Set TMDS Character Rate to Above 340 Mcsc Set TMDS Character Rate to Above 340 Mcsc
Set Up	TMDS Character Rate <= 165 Mcsc	PixelClockV100	0.0, 1.0	Set TMDS Character Rate to Below 165Mcscz Set TMDS Character Rate to Below 165Mcsc
Set Up	Test Mode	TestMode	Compliance Mode, Debug Mode	Determine whether compliance or debug mode
Set Up	chkOffline	chkOffline	0.0, 1.0	chkOffline
*Limited availability: Availability of this setting depends upon the oscilloscope model and installed license options.				

3 Test Names and IDs

The following table shows the mapping between each test's numeric ID and name. The numeric ID is required by various remote interface methods.

- Name – The name of the test as it appears on the user interface **Select Tests** tab.
- Test ID – The number to use with the RunTests method.
- Description – The description of the test as it appears on the user interface **Select Tests** tab.

For example, if the graphical user interface displays this tree in the **Select Tests** tab:

- All Tests
  - Rise Time
  - Fall Time

then you would expect to see something like this in the table below:

Table 3 Example Test Names and IDs

Name	Test ID	Description
Fall Time	110	Measures clock fall time.
Rise Time	100	Measures clock rise time.

and you would run these tests remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SelectedTests '100,110'"
arsl -a ipaddress -c "Run"

C# syntax
---------
remoteAte.SelectedTests = new int[]{100,110};
remoteAte.Run();
```

Here are the actual Test names and IDs used by this application:

NOTE The file, ""TestInfo.txt"", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 4 Test IDs and Names

Name	TestID	Description
1-1: VL Clock +	7030000	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
1-1: VL Clock -	7040000	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
1-1: VL D0+	7050000	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
1-1: VL D0-	7060000	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
1-1: VL D1+	7070000	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
1-1: VL D1-	7080000	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
1-1: VL D2+	7090000	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
1-1: VL D2-	7010000	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
1-2: Clock Fall Time	2010000	2 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
1-2: Clock Rise Time	2000000	2 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
1-2: D0 Fall Time	2030000	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
1-2: D0 Rise Time	2020000	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
1-2: D1 Fall Time	2050000	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1-2: D1 Rise Time	2040000	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
1-2: D2 Fall Time	2070000	Confirm that the rise times and fall times on the TMDS differential signals fall within the limits of the specification.
1-2: D2 Rise Time	2060000	Confirm that the rise times and fall times on the TMDS differential signals fall within the limits of the specification.
1-4: Intra-Pair Skew - Clock	6000000	Confirm that any skew within any one differential data pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.
1-4: Intra-Pair Skew - Data Lane 0	6010000	Confirm that any skew within any one differential data pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.
1-4: Intra-Pair Skew - Data Lane 1	6040000	Confirm that any skew within any one differential data pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.
1-4: Intra-Pair Skew - Data Lane 2	6050000	Confirm that any skew within any one differential data pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.
1-5: Clock Duty Cycle(Maximum)	5020000	2 Channels Connection Model:Confirm that the duty cycle of the differential TMDS clock does not exceed the limits allowed by the specification. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
1-5: Clock Duty Cycle(Minimum)	5010000	2 Channels Connection Model: Confirm that the duty cycle of the differential TMDS clock does not exceed the limits allowed by the specification. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
1-6: Clock Jitter	1200000	2 Channels Connection Model: TMDS differential clock jitter must not exceed 0.27*Tbit, relative to the ideal Recovery Clock. For compliance, the DUT should output > 340MHz for testing.
1-7: D0 Mask Test (TP8_EQ with Worst Case Skew)	3200000	Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
1-7: D0 Mask Test (TP8_EQ)	2200000	Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
1-7: D1 Mask Test (TP8_EQ with Worst Case Skew)	3400000	Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
1-7: D1 Mask Test (TP8_EQ)	2400000	Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
1-7: D2 Mask Test (TP8_EQ with Worst Case Skew)	3600000	Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
1-7: D2 Mask Test (TP8_EQ)	2600000	Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
7-10: D0 Data Jitter	3	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D0 Data Jitter Separation	9	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D0 Mask Test	2	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D1 Data Jitter	5	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D1 Data Jitter Separation	10	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D1 Mask Test	4	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D2 Data Jitter	7	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D2 Data Jitter Separation	90	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: D2 Mask Test	6	For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.
7-10: Eye Pattern (Required For All Pixel Rates)	9004	

Table 4 Test IDs and Names (continued)

Name	TestID	Description
7-2: VL Clock +	73	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL Clock +	703	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL Clock -	74	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL Clock -	704	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL D0+	75	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL D0+	705	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL D0-	76	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL D0-	706	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL D1+	77	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL D1+	707	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
7-2: VL D1-	78	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL D1-	708	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL D2+	79	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL D2+	709	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL D2-	71	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-2: VL D2-	701	The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-3: Voff Clock +	713	Confirm that a disabled TMDS link only allows leakage currents within specified limits.
7-3: Voff Clock -	714	Confirm that a disabled TMDS link only allows leakage currents within specified limits.
7-3: Voff D0+	715	Confirm that a disabled TMDS link only allows leakage currents within specified limits.
7-3: Voff D0-	716	Confirm that a disabled TMDS link only allows leakage currents within specified limits.
7-3: Voff D1+	717	Confirm that a disabled TMDS link only allows leakage currents within specified limits.
7-3: Voff D1-	718	Confirm that a disabled TMDS link only allows leakage currents within specified limits.
7-3: Voff D2+	719	Confirm that a disabled TMDS link only allows leakage currents within specified limits.
7-3: Voff D2-	711	Confirm that a disabled TMDS link only allows leakage currents within specified limits.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
7-4: Clock Fall Time	201	2 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-4: Clock Rise Time	200	2 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-4: D0 Fall Time	203	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-4: D0 Rise Time	202	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-4: D1 Fall Time	205	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-4: D1 Rise Time	204	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-4: D2 Fall Time	207	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-4: D2 Rise Time	206	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-4: Transition Time (Required For The Highest Supported Pixel Rate)	9005	
7-5: Clock - Overshoot	400	2 Channels Connection Model: TMDS overshoot must be below 15% of 2*VSWING. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-5: Clock - Undershoot	401	2 Channels Connection Model: TMDS undershoot must below 25% of 2*VSWING. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
7-5: D0 - Overshoot	402	TMDS overshoot must be below 15% of 2*VSWING. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-5: D0 - Undershoot	403	TMDS undershoot must below 25% of 2*VSWING. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-5: D1 - Overshoot	404	TMDS overshoot must be below 15% of 2*VSWING. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-5: D1 - Undershoot	405	TMDS undershoot must below 25% of 2*VSWING. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-5: D2 - Overshoot	406	TMDS overshoot must be below 15% of 2*VSWING. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-5: D2 - Undershoot	407	TMDS undershoot must below 25% of 2*VSWING. For compliance, the DUT should output the lowest supported pixel clock frequency during the test.
7-6: Inter-Pair Skew (Required For The Highest Supported Pixel Rate)	9009	
7-6: Inter-Pair Skew - D0/Clock	330	Inter-pair skew must not exceed 0.20*Tpixel. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-6: Inter-Pair Skew - D0/D1	300	Inter-pair skew must not exceed 0.20*Tpixel. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-6: Inter-Pair Skew - D0/D2	302	Inter-pair skew must not exceed 0.20*Tpixel. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-6: Inter-Pair Skew - D1/Clock	331	Inter-pair skew must not exceed 0.20*Tpixel. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-6: Inter-Pair Skew - D1/Clock	332	Inter-pair skew must not exceed 0.20*Tpixel. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
7-6: Inter-Pair Skew - D1/D2	301	Inter-pair skew must not exceed 0.20*Tpixel. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-6: Single Ended Test (Required For The Highest Supported Pixel Rate)	9008	
7-7: Intra-Pair Skew - Clock	600	Frequency > 165 MHz: Intra-Pair Skew must not exceed 0.15*Tbit. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-7: Intra-Pair Skew - Clock	60	Frequency < 165 MHz : Intra-Pair Skew must not exceed 0.15*Tbit. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-7: Intra-Pair Skew - Data Lane 0	601	Frequency > 165 MHz: Intra-Pair Skew must not exceed 0.15*Tbit. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-7: Intra-Pair Skew - Data Lane 0	61	Frequency < 165 MHz: Intra-Pair Skew must not exceed 0.15*Tbit. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-7: Intra-Pair Skew - Data Lane 1	604	Frequency > 165 MHz: Intra-Pair Skew must not exceed 0.15*Tbit. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-7: Intra-Pair Skew - Data Lane 1	64	Frequency < 165 MHz: Intra-Pair Skew must not exceed 0.15*Tbit. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-7: Intra-Pair Skew - Data Lane 2	605	Frequency > 165 MHz: Intra-Pair Skew must not exceed 0.15*Tbit. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
7-7: Intra-Pair Skew - Data Lane 2	65	Frequency < 165 MHz: Intra-Pair Skew must not exceed 0.15*Tbit. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-8: Clock Duty Cycle (Required For The Highest Supported Pixel Rate)	9007	
7-8: Clock Duty Cycle(Maximum)	502	2 Channels Connection Model: Clock duty cycle must be at least 40% and not more than 60%.The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-8: Clock Duty Cycle(Minimum)	501	2 Channels Connection Model: Clock duty cycle must be at least 40% and not more than 60%.The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
7-9: Clock Jitter	12	2 Channels Connection Model: TMDS differential clock jitter must not exceed 0.25*Tbit, relative to the ideal Recovery Clock. For compliance, the DUT should output 27MHz(or 25MHz), 74.25MHz, 148.5MHz, and 222.75MHz for testing.
7-9: Clock Jitter (Required For All Pixel Rates)	9003	
Cable Clock Jitter	85	TMDS differential clock jitter must not exceed 0.25*Tbit, relative to the ideal Recovery Clock. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
Cable Clock Jitter	1085	TMDS differential clock jitter must not exceed 0.25*Tbit, relative to the ideal Recovery Clock. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
Cable Data Jitter	83	Eye diagram Data Jitter with equalized clock,data and Transition Time Converter using coefficients store in file
Cable Inter-Pair Skew	86	Cable Assembly Inter-Pair Skew should be no more than 2.42ns.
Cable Inter-Pair Skew - D0/D1	1086	Cable Assembly Inter-Pair Skew should be no more than 2.42ns.
Cable Inter-Pair Skew - D0/D2	1186	Cable Assembly Inter-Pair Skew should be no more than 2.42ns.
Cable Inter-Pair Skew - D1/D2	1286	Cable Assembly Inter-Pair Skew should be no more than 2.42ns.
Cable Intra-Pair Skew	87	Cable Assembly Intra-Pair Skew should be no more than 151ps.
Cable Mask Test	84	Eye diagram Mask Test with equalized clock,data and Transition Time Converter using coefficients store in file

Table 4 Test IDs and Names (continued)

Name	TestID	Description
D0 Cable Data Jitter	1083	Eye diagram Data Jitter with equalized clock,data and Transition Time Converter using coefficients store in file
D0 Cable Intra-Pair Skew	1087	Cable Assembly Intra-Pair Skew should be no more than 151ps.
D0 Cable Mask Test	1084	Eye diagram Mask Test with equalized clock,data and Transition Time Converter using coefficients store in file
D0 Data Jitter Separation (TP2_EQ with Worst Case Negative Skew)	400001	The Source shall have output levels at TP2, which meet the normalized eye diagram requirements.
D0 Data Jitter Separation (TP2_EQ with Worst Case Positive Skew)	400000	The Source shall have output levels at TP2, which meet the normalized eye diagram requirements.
D1 Cable Data Jitter	1183	Eye diagram Data Jitter with equalized clock,data and Transition Time Converter using coefficients store in file
D1 Cable Intra-Pair Skew	1187	Cable Assembly Intra-Pair Skew should be no more than 151ps.
D1 Cable Mask Test	1184	Eye diagram Mask Test with equalized clock,data and Transition Time Converter using coefficients store in file
D1 Data Jitter Separation (TP2_EQ with Worst Case Negative Skew)	400003	The Source shall have output levels at TP2, which meet the normalized eye diagram requirements.
D1 Data Jitter Separation (TP2_EQ with Worst Case Positive Skew)	400002	The Source shall have output levels at TP2, which meet the normalized eye diagram requirements.
D2 Cable Data Jitter	1283	Eye diagram Data Jitter with equalized clock,data and Transition Time Converter using coefficients store in file
D2 Cable Intra-Pair Skew	1287	Cable Assembly Intra-Pair Skew should be no more than 151ps.
D2 Cable Mask Test	1284	Eye diagram Mask Test with equalized clock,data and Transition Time Converter using coefficients store in file
D2 Data Jitter Separation (TP2_EQ with Worst Case Negative Skew)	400005	The Source shall have output levels at TP2, which meet the normalized eye diagram requirements.
D2 Data Jitter Separation (TP2_EQ with Worst Case Positive Skew)	400004	The Source shall have output levels at TP2, which meet the normalized eye diagram requirements.
HEC Eye Diagram Test (Differential Mode)	2010	To evaluate eye diagram of HEC differential signals.
HF1-1: D0+ VSwing	70501	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: D0- VSwing	70601	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: D1+ VSwing	70701	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: D1- VSwing	70801	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
HF1-1: D2+ VSwing	70901	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: D2- VSwing	70101	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: VL Clock +	70300	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: VL Clock -	70400	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: VL D0+	70500	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: VL D0-	70600	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: VL D1+	70700	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: VL D1-	70800	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: VL D2+	70900	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1: VL D2-	70100	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1:Clock + VSwing	70301	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-1:Clock - VSwing	70401	Confirm that the DC voltage levels on the HDMI link are within the specified limits for each TMDS signal.
HF1-2: Clock Fall Time	20100	2 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
HF1-2: Clock Rise Time	20000	2 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
HF1-2: D0 Fall Time	20300	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
HF1-2: D0 Rise Time	20200	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
HF1-2: D1 Fall Time	20500	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
HF1-2: D1 Rise Time	20400	The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
HF1-2: D2 Fall Time	20700	Confirm that the rise times and fall times on the TMDS differential signals fall within the limits of the specification.
HF1-2: D2 Rise Time	20600	Confirm that the rise times and fall times on the TMDS differential signals fall within the limits of the specification.
HF1-3: Inter-Pair Skew - D0/D1	30000	Confirm that any skew between the differential data pairs in the TMDS portion of the HDMI link does not exceed the limits in the specification.
HF1-3: Inter-Pair Skew - D0/D2	30200	Confirm that any skew between the differential data pairs in the TMDS portion of the HDMI link does not exceed the limits in the specification.
HF1-3: Inter-Pair Skew - D1/D2	30100	Confirm that any skew between the differential data pairs in the TMDS portion of the HDMI link does not exceed the limits in the specification.
HF1-4: Intra-Pair Skew - Clock	60000	Confirm that any skew within any one differential data pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.
HF1-4: Intra-Pair Skew - Data Lane 0	60100	Confirm that any skew within any one differential data pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.
HF1-4: Intra-Pair Skew - Data Lane 1	60400	Confirm that any skew within any one differential data pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.
HF1-4: Intra-Pair Skew - Data Lane 2	60500	Confirm that any skew within any one differential data pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.
HF1-5: D0 Maximum Differential Voltage	22000	Confirm that the differential signal on each TMDS differential data pair does not exceed Maximum/Minimum Differential Voltage.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
HF1-5: D0 Minimum Differential Voltage	22001	Confirm that the differential signal on each TMDS differential data pair does not exceed Maximum/Minimum Differential Voltage.
HF1-5: D1 Maximum Differential Voltage	24000	Confirm that the differential signal on each TMDS differential data pair does not exceed Maximum/Minimum Differential Voltage.
HF1-5: D1 Minimum Differential Voltage	24001	Confirm that the differential signal on each TMDS differential data pair does not exceed Maximum/Minimum Differential Voltage.
HF1-5: D2 Maximum Differential Voltage	26000	Confirm that the differential signal on each TMDS differential data pair does not exceed Maximum/Minimum Differential Voltage.
HF1-5: D2 Minimum Differential Voltage	26001	Confirm that the differential signal on each TMDS differential data pair does not exceed Maximum/Minimum Differential Voltage.
HF1-6: Clock Duty Cycle(Maximum)	50200	Confirm that the duty cycle of the differential TMDS clock does not exceed the limits allowed by the specification. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
HF1-6: Clock Duty Cycle(Minimum)	50100	Confirm that the duty cycle of the differential TMDS clock does not exceed the limits allowed by the specification. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
HF1-6: Clock Rate	50300	Confirm that the duty cycle of the differential TMDS clock does not exceed the limits allowed by the specification. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
HF1-7: Clock Jitter (TP2_EQ with Worst Case Negative Skew)	12001	2 Channels Connection Model: TMDS differential clock jitter must not exceed 0.3*Tbit, relative to the ideal Recovery Clock. For compliance, the DUT should output > 340MHz for testing.
HF1-7: Clock Jitter (TP2_EQ with Worst Case Positive Skew)	12000	2 Channels Connection Model: TMDS differential clock jitter must not exceed 0.3*Tbit, relative to the ideal Recovery Clock. For compliance, the DUT should output > 340MHz for testing.
HF1-7: Clock Jitter (TP2_EQ)	12002	2 Channels Connection Model: TMDS differential clock jitter must not exceed 0.3*Tbit, relative to the ideal Recovery Clock. For compliance, the DUT should output > 340MHz for testing.
HF1-7: Differential Clock Voltage Swing, Vs (TP1)	12003	This is a subset of the clock jitter test where the differential voltage swing at TP1 must be > 400mV and < 1200mV.
HF1-8: D0 Mask Test (TP1)	32003	Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D0 Mask Test (TP2_EQ with Worst Case Negative Skew)	32001	Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
HF1-8: D0 Mask Test (TP2_EQ with Worst Case Positive Skew)	32000	Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D0 Mask Test (TP2_EQ)	32002	Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D1 Mask Test (TP1)	34003	Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D1 Mask Test (TP2_EQ with Worst Case Negative Skew)	34001	Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D1 Mask Test (TP2_EQ with Worst Case Positive Skew)	34000	Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D1 Mask Test (TP2_EQ)	34002	Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D2 Mask Test (TP1)	36003	Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D2 Mask Test (TP2_EQ with Worst Case Negative Skew)	36001	Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D2 Mask Test (TP2_EQ with Worst Case Postive Skew)	36000	Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
HF1-8: D2 Mask Test (TP2_EQ)	36002	Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) that meets or exceeds the limits on eye opening in the specification.
Receiver Clock Jitter	82	TMDS differential clock jitter must not exceed 0.25*Tbit, relative to the ideal Recovery Clock. For compliance, the DUT should output the highest supported pixel clock frequency during the test.
Receiver Equalized Eye Diagram	80	Eye diagram with equalized clock and data using coefficients store in file.
Receiver Equalized Jitter Separation	81	Jitter Separation with equalized clock and data using coefficients store in file.
Save Clock Waveform (TP2_EQ with Worst Case Positive Skew)	88010	Saves waveforms for clock lanes.
Save Lane D0 Waveform (TP1)	88000	Saves waveforms for clock lanes.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Test ID 5-11: ARC Operating DC Voltage (Single Mode)	3950	To evaluate operating DC voltage of ARC Single Mode signals.
Test ID 5-12: ARC Signal Amplitude (Single Mode)	4000	To evaluate signal Amplitude of Single Mode ARC signals.
Test ID 5-13a: ARC Rise Time (Single Mode)	4014	To evaluate rise time of HDMI ARC Single Mode signal.
Test ID 5-13b: ARC Fall Time (Single Mode)	4015	To evaluate fall time of HDMI ARC Single Mode signal.
Test ID 5-14a: ARC Jitter Test(Single Mode)	4020	To evaluate total jitter of ARC signals.
Test ID 5-14b: ARC Clock Frequency (Single Mode)	4030	To evaluate clock frequency of HDMI ARC Single Mode signal.
Test ID 5-19: ARC Rx Operating DC Voltage(Common Mode)	3050	To evaluate operating DC voltage of ARC signals for receiver.
Test ID 5-1: HEC Operating DC Voltage	1900	To evaluate operating DC voltage of HEC differential signals.
Test ID 5-2 HEC Maximum Jitter Test (Differential Mode)	2011	To evaluate maximum jitter of HEC differential signals.
Test ID 5-20: ARC Operating DC Voltage For Receiver(Single Mode)	4050	To evaluate operating DC voltage of ARC Single Mode signals for receiver.
Test ID 5-3a: HEC Rise Time Test Top(Differential Mode)	2020	To evaluate rise time of top MLT-3 differential mode signal of HDMI HEC transmission.
Test ID 5-3b: HEC Fall Time Test Top(Differential Mode)	2021	To evaluate fall time of top MLT-3 differential mode signal of HDMI HEC transmission.
Test ID 5-3c:HEC Rise Time Test Bottom(Differential Mode)	2022	To evaluate rise time of Bottom MLT-3 differential mode signal of HDMI HEC transmission.
Test ID 5-3d:HEC Fall Time Test Bottom(Differential Mode)	2023	To evaluate fall time of bottom MLT-3 differential mode signal of HDMI HEC transmission.
Test ID 5-4a: HEC High Level Voltage (Differential Mode)	2000	To evaluate high level voltage of HEC differential signals.
Test ID 5-4b: HEC Low Level Voltage (Differential Mode)	2001	To evaluate low level voltage of HEC differential signals.
Test ID 5-4c: HEC Center Level Voltage (Differential Mode)	2002	To evaluate center level voltage of HEC differential signals.
Test ID 5-5a:HEC Cycle Time Top (Differential Mode)	2030	To evaluate cycle time of differential mode signal of HDMI HEC transmission.
Test ID 5-5b: HEC Cycle Time Bottom (Differential Mode)	2031	To evaluate cycle time of differential mode signal of HDMI HEC transmission.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Test ID 5-6: ARC Operating DC Voltage (Common Mode)	2950	To evaluate operating DC voltage of ARC signals.
Test ID 5-7a: ARC High Level Voltage (Common Mode)	3000	To evaluate high level voltage of ARC signals.
Test ID 5-7b: ARC Low Level Voltage (Common Mode)	3001	To evaluate low level voltage of ARC signals.
Test ID 5-8a: ARC Rise Time (Common Mode)	3014	To evaluate rise time of HDMI ARC Common mode signal.
Test ID 5-8b: ARC Fall Time (Common Mode)	3015	To evaluate fall time of HDMI ARC Common mode signal.
Test ID 5-8c: ARC Rise Time (Common Mode with HEC)	3016	To evaluate rise time of HDMI ARC Common mode signal when HEC accompanies ARC.
Test ID 5-8d: ARC Fall Time (Common Mode with HEC)	3017	To evaluate fall time of HDMI ARC Common mode signal when HEC accompanies ARC.
Test ID 5-9a: ARC Jitter Test(Common Mode)	3020	To evaluate total jitter of ARC signals.
Test ID 5-9b: ARC Clock Frequency (Common Mode)	3030	To evaluate clock frequency of HDMI ARC Common mode signal.

4 Instruments

The following table shows the instruments used by this application. The name is required by various remote interface methods.

- Instrument Name — The name to use as a parameter in remote interface commands.
- Description — The description of the instrument.

For example, if an application uses an oscilloscope and a pulse generator, then you would expect to see something like this in the table below:

Table 5 Example Instrument Information

Name	Description
scope	The primary oscilloscope.
Pulse	The pulse generator used for Gen 2 tests.

and you would be able to remotely control an instrument using:

```
ARSL syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
arsl -a ipaddress -c "SendScpiCommandCustom 'Command=[scpi
command];Timeout=100;Instrument=pulsegen'"

arsl -a ipaddress -c "SendScpiQueryCustom 'Command=[scpi
query];Timeout=100;Instrument=pulsegen'"


C# syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
SendScpiCommandOptions commandOptions = new SendScpiCommandOptions();
commandOptions.Command = "[scpi command]";
commandOptions.Instrument = "[instrument name]";
commandOptions.Timeout = [timeout];
remoteAte.SendScpiCommand(commandOptions);

SendScpiQueryOptions queryOptions = new SendScpiQueryOptions();
queryOptions.Query = "[scpi query]";
queryOptions.Instrument = "[instrument name]";
```

```
queryOptions.Timeout = [timeout];
remoteAte.SendScpiQuery(queryOptions);
```

Here are the actual instrument names used by this application:

NOTE The file, ""InstrumentInfo.txt"", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 6 Instrument Names

Instrument Name	Description
scope	The primary oscilloscope

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